Past Papers Questions:

Section 3.3: Computer Architectures and the Fetch-Execute Cycle

May/June 2003

4 The next instruction to be carried out is

LDAN 25

which loads the number 25 into the accumulator.
With reference to the special registers in a processor, describe the stages of the fetch-execute cycle when dealing with this instruction. [6]

October / November 2003

5 Describe the fetch/decode/execute/reset cycle when an ADD instruction is being executed.
You should include
_ Program Counter (PC)
_ Memory Address Register (MAR)
_ Memory Data Register (MDR)
_ Current Instruction Register (CIR)
_ Accumulator
in your answer. [7]

May/June 2004

3 (a) Describe what is meant by Von Neumann architecture. [3]

(b) Explain the purpose of each of the following special registers in a processor.
(i) Program Counter (Sequence Control Register). [2]
(ii) Current Instruction Register. [2]
(iii) Memory Address Register. [2]
(iv) Memory Data Register. [2]
(v) Accumulator. [2]

October/November 2004

5 (a) Describe the stages of the fetch/decode/execute/reset cycle, explaining how the special registers in the processor are used. You should use as an example the processing of a jump instruction. [9]

(b)
(i) Explain what is meant by a parallel processing system. [1]
(ii) Give an advantage and a disadvantage of parallel processing as opposed to serial processing. [2]

8 (b) Explain the need for parallel architecture when using a computer to forecast the weather. [3]

May/June 2005

2 JUMP 300 is an instruction to be executed by a processor. It means that the next instruction the processor should process is held in location 300.
Describe the stages of the fetch/decode/execute cycle and the effects on the contents of the registers in the processing of this instruction. [7]

9 Discuss the need for parallel architecture when processing some simulations. [4]

October/November 2005

4 A processor is to carry out the instruction ADD 200. This instruction means that the contents of memory location 200 should be added to the accumulator.

Describe the steps of the fetch-execute cycle, stating the effect on the registers in the processor, when carrying out this instruction. [8]

May/June 2006

5 Describe the fetch/decode/execute/reset cycle when the next instruction to be executed is an unconditional jump instruction. [7]

October/November 2006

1 (a) Describe the purpose of the following registers in a processor:
(i) Current instruction register (CIR), [2]
(ii) Memory address register (MAR), [2]
(iii) Program counter (PC), [2]
(iv) Index register (IR). [2]

(b) (i) Explain how a parallel processor system differs from a sequential processor system. [2]
(ii) Give an example of an application for which it would be sensible to use parallel processing, justifying your choice. [2]

May/June 2007

7 (a) Describe what is meant by Von Neumann architecture. [2]
(b) (i) Explain how parallel processing differs from serial processing. [2]
(ii) State an application which would use parallel processing, giving a reason for your answer. [2]

October/November 2007

8 (a) Using an example application, explain why some applications require parallel processing rather than serial processing. [3]
(b) Describe what is needed to run a parallel process rather than a serial process. [3]

May/June 2008

6 (a) (i) State what is held in the Program Counter (PC) during the fetch/execute cycle. [1]
(ii) Explain how the contents of the PC change during the fetch/execute cycle. [4]
(b) Describe the contents of the memory address register (MAR) during the fetch/execute cycle. [4]